SEMICONDUCTOR DEVICE INCLUDING TWO-DIMENSIONAL MATERIAL

[0001] CROSS-REFERENCE TO RELATED APPLICATION(S)

[0002] This application claims priority from Korean Patent Application No. 10-2015-0144946, filed on Oct. 16, 2015, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein by reference in its entirety.

BACKGROUND

[0003] 1. Field

[0004] The exemplary embodiments disclosed herein relate to a semiconductor device, and more particularly, to a semiconductor device including a two-dimensional (2D) material.

[0005] 2. Description of Related Art

[0006] A two-dimensional (2D) material is a single-layered solid of atoms having a predetermined crystal structure, and graphene is a representative 2D material. Graphene has a monoatomic layer structure in which carbon atoms form a hexagonal structure. Graphene may have a symmetrical band structure on the basis of a Dirac point, and since an effective mass of electric charges at the Dirac point is very small, the graphene may have a charge mobility at least ten times (significantly thousands times or more) greater than that of silicon (Si). Further, graphene may have a very large Fermi velocity. Such graphene has entered the spotlight as a next-generation material that can overcome limitations of existing devices, and by starting research on such graphene, research and development on various 2D materials having insulating or semiconductor characteristics have been conducted.

[0007] A large number of semiconductor devices including 2D materials include P-N junctions formed by at least 2D material. There are several structures and/or methods for forming the P-N junction of the 2D material, and the following ways are representative thereof. The first method is a method of forming a P-N junction by partially inducing P-type region and N-type region in a 2D material layer through an electrical gating in a state in which a double gating structure is formed on a back surface of a substrate, on which the 2D material layer is formed. The second method, which is a method using chemical doping, is a method of forming a P-N junction by inducing a P-type or N-type material in a portion of a 2D material layer. In this case, an N-type or P-type material may be induced in the other portions of the 2D material layer if necessary. The third method is a method of forming a P-N junction by bonding a P-type material to an N-type material, and both sides may be 2D materials, or one side may be a bulk material and the other may be a 2D material.

[0008] However, such a P-N junction using an existing 2D material has a complex structure in which two different voltages should be applied, is difficult to ensure controllability or reproducibility thereof, or uses different types of materials as a P-type material and an N-type material, and thus an interface issue may be caused.

SUMMARY

[0009] This summary is provided to introduce a selection of concepts in a simplified form that are further described below in the Detailed Description. This summary is not intended to identify key features or essential features of the claimed subject matter, nor is it intended to be used as an aid in determining the scope of the claimed subject matter.

[0010] The exemplary embodiments disclosed herein may provide a semiconductor device including a two-dimensional (2D) material having a simple structure and not having any interface issues.

[0011] The exemplary embodiments disclosed herein may also provide a semiconductor device including a 2D material having excellent electric or physical characteristics and not having any interface issues.

[0012] The exemplary embodiments disclosed herein may further provide a semiconductor device including a 2D material having a reversible P-N diode characteristic.

[0013] According to an aspect of an exemplary embodiment, there is provided a semiconductor device including: a substrate; a two-dimensional (2D) material layer formed on the substrate and having a first region and a second region adjacent to the first region; and a source electrode and a drain electrode provided to be respectively in contact with the first region and the second region of the 2D material layer, wherein the second region of the 2D material layer includes an oxygen adsorption material layer in which oxygen is adsorbed on a surface of the second region.

[0014] A difference between a work function of the oxygen adsorption material layer and a work function of the 2D material layer in the first region may be 0.3 eV or more.

[0015] The 2D material layer may be formed of MoS_2.

[0016] An oxygen adsorption rate of the oxygen adsorption material layer formed on the surface of the second region of the 2D material layer may be 2% or more.

[0017] The oxygen adsorption rate of the oxygen adsorption material layer formed on the surface of the second region of the 2D material layer may be in a range of 2% to 30%.

[0018] The source electrode and the drain electrode are formed of different materials.

[0019] One electrode among the source and drain electrodes is formed of Cr or Au and the other electrode among the source and drain electrodes is formed of Pd.

[0020] The semiconductor device may further include a passivation layer formed to cover the first region of the 2D material layer.

[0021] The passivation layer may be formed of an insulating material configured to prevent oxygen from penetrating a surface of the first region.

[0022] According to an aspect of another exemplary embodiment, there is provided a semiconductor device including a multi-layered structure, the device including: a semiconductor layer formed of a 2D material and having a first region and a second region, wherein the semiconductor layer includes an oxygen adsorption material layer in which oxygen is adsorbed on a surface of the 2D material in the second region; and a non-semiconductor layer provided on a surface of the semiconductor layer.

[0023] The semiconductor device may be a tunneling device, and the semiconductor layer may be a tunneling layer.

[0024] The semiconductor device may be a binary junction transistor (BJT), and the semiconductor layer may be a tunneling layer.

[0025] The semiconductor device may be a barristor, and the semiconductor layer may be a channel layer.